

Appl. No. 10/709,427  
Amdt. dated January 16, 2006  
Reply to Office action of November 08, 2005

### REMARKS/ARGUMENTS

#### 1. Objection to the specification:

The specification is objected to because it does not identify Fig. 4's element 50.

5 The specification is objected to for describing Figs. 4-5's elements 52 as "lead frames".

The specification is objected to for describing Fig. 6's elements 98 as "lead frames" Correction is required.

#### Response:

10 Paragraphs [0005] and [0021] of the specification have been amended to overcome the objections to the specification. Element 50 in Fig. 4 is now described in paragraph [0021] of the disclosure, and other grammatical errors have also been corrected.

15 Although Figures 4 and 6 of the instant application appear similar to Figures 2A and 2B of Lau et al, there are differences in the parts illustrated in the respective figures. Lau illustrates in Figures 2A and 2B a lead frame that contains many leads 203, a die attach pad 202, and a die 206. Lau's lead frame corresponds to the bonding option architecture 50 without bonding wires 54 and the chip 56 as shown  
20 in Figure 4, and Lau's leads 203 correspond to the claimed lead frames. In addition, Lau's die attach pad 202 correspond to one of the claimed package substrates. Therefore, the applicant submits that the specification correctly describes with respect to Figures 4-6 that a plurality of lead frames 52 and 98 surround the package substrates. Acceptance of the amended specification is respectfully requested.

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#### 2. Objection to claim 1:

Claim 1 is objected to because "the bonding pads" lack antecedent basis.

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Response:

Claim 1 has been amended to overcome this objection.

5 3. Rejection of claims 1-8 under 35 U.S.C. 112, first paragraph:

Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement. The claimed first and second package substrates are unclear, particularly in the absence of cross-sectional and/or perspective views thereof.

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Response:

As explained above with respect to the specification, the chip packaging structures illustrated in Figures 4 and 6 contain two different package substrates. Each of the package substrates having a different voltage level can be connected to a bonding option pad for allowing the bonding option pad to receive the different voltage levels. Figure 4 shows that a second package substrate 60 surrounds a first package substrate 58 on both the inner and outer sides of the first package substrate 58. Figure 6 shows that a second package substrate 92 surrounds a first package substrate 90 on the outer side of the first package substrate 90. The applicant therefore submits that the claimed first and second package substrates are clearly described in the disclosure, and reconsideration of claims 1-8 is respectfully requested.

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4. Rejection of claims 1-8 under 35 U.S.C. 102(e):

25 Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lau et al. (US 6,822,319, hereinafter Lau) for reasons of record.

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Claim 1 has been amended to overcome this rejection. Claim 1 now recites each of a first and second package substrate has a high or a low voltage, and the voltage level of the first package substrate is the logical opposite of the voltage level of the second package substrate. Furthermore, claim 1 recites that each bonding option pad of the chip is selectively connected to the first package substrate or the second package substrate. No new matter is added through these amendments to claim 1.

Lau teaches a process for enhancing visual detectability of a lead frame by plating at least one of a ring, a line and an array of dots on the die attach pad of the lead frame. However, Lau does not teach the bonding options by the first or second package substrate having different voltage levels.

Moreover, Lau teaches in column 3, lines 32-34 that silver plating is applied in an array of dots or in a ring around the periphery of the die attach pad 202. Therefore, Lau's two rings that are shown are formed out of conductive silver plating, and do not constitute first and second package substrates. Furthermore, Lau does not teach two package substrates (which correspond to the die attach pad in Lau's invention) having different voltage levels. For these reasons, Lau does not teach that bonding option pads of the chip selectively connect to the first package substrate or the second package substrate. Since Lau does not teach all of the claimed limitations contained in the currently amended claim 1, claim 1 is patentable over the cited prior art. Claims 3-8 are dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 1 and 3-8 is respectfully requested.

5. Introduction to new claims 19 and 20:

New claim 19 further narrows claim 5 and specifies that a pin connected to a lead is connected to an input/output signal. No new matter is added through this claim.

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New claim 20 specifies that each bonding option pad of the chip has a corresponding lead frame, and can be selectively connected to the first package substrate, the second package substrate, or the corresponding lead frame. This amendment is fully supported in paragraph [0024] of the specification and in Figure 5. No new matter is added through this amendment.

By providing the option of connecting each bonding option pad to the corresponding lead or either of the two package substrates, greater flexibility is offered for connecting the bonding option pad to different voltage levels or input/output signals.

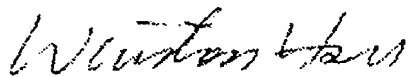
On the other hand, Lau teaches in Fig. 2A and Fig. 2B that the chip 206 has approximately 60 bonding pads, but only has 32 leads on the chip packaging. Therefore, Lau does not teach that each bonding option pad can have a corresponding lead, as is claimed in the new claim 20. Because of this, Lau does not provide the structure necessary for selectively connecting each bonding pad to a corresponding lead or to either of two package substrates since there are not enough leads to be used for each of the bonding pads.

Acceptance of new claims 19 and 20 is respectfully requested.

In light of the above statements in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



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is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)